

Staff Name:

Lab/Prog/Dept:

HOD:

Appraisal Period: Jan to Dec 2012

Project/Assignment Name	RO for this Project	Expected End Date of Project	% time spent on Project
GaN-on-Si MOCVD growth	Patrick Lo	30-Dec-12	20
GaN-on-Si HEMT process development	Patrick Lo	30-Aug-12	20
GaN-on-Si device modelling and PDK	Patrick Lo	30-Jun-13	20
Rolls Royce GaN feasibility study	Patrick Lo	30-Jul-12	20
Huawei Characterization project	Patrick Lo	30-Jul-12	20

Key Deliverables (descriptive only) for 2012	Progress on Deliverables
<ul style="list-style-type: none"> <li>- Complete installation of GaN-on-Si MOCVD system</li> <li>- Complete GaN-on-Si MOCVD growth on 200 mm substrates</li> <li>- Develop CMOS compatible GaN-on-Si HEMT</li> </ul>	<ul style="list-style-type: none"> <li>- working with facilities hook-up contractor and Veeco to complete MOCVD installation</li> <li>- will start growth experiments in Aug 12</li> </ul>
<ul style="list-style-type: none"> <li>- Develop process for CMOS compatible GaN HEMT devices</li> </ul>	<ul style="list-style-type: none"> <li>- Process development underway, completed GaN etching, and different shortloops for module development</li> </ul>
<ul style="list-style-type: none"> <li>- Characterize active and passive devices fabricated from NTU</li> <li>- Develop device models from characterization data</li> <li>- Implement device models into process design kit (PDK)</li> <li>- Design millimeter wave power amplifier circuit using PDK</li> </ul>	<ul style="list-style-type: none"> <li>- currently characterizing NTU devices</li> </ul>
<ul style="list-style-type: none"> <li>- submit paper which studies technical and market feasibility of using GaN transistors in power electronic applications</li> <li>- Complete circuit simulations of power inverters which compare the performance of GaN transistor power switches versus Si and SiC transistor power switches</li> </ul>	<ul style="list-style-type: none"> <li>- feasibility paper submitted to Rolls Royce</li> <li>- first iterations of thermal and circuit simulations complete</li> <li>- first iteration of thermal cooling design complete</li> </ul>
<ul style="list-style-type: none"> <li>- Complete DC characterization measurements of MOSFET transistors</li> <li>- Complete RF measurements and models of Balun devices</li> <li>- Complete load pull measurements of cascode circuit</li> </ul>	<ul style="list-style-type: none"> <li>- Characterization of MOSFET transistors mostly complete</li> <li>- measurements of balun devices mostly complete need to take 2-port measurements and create models</li> <li>- load pull measurements not started yet</li> </ul>



IP (1st Inventor) Disclosed	IP (1st Inventor) Filed	No of PhD Student Attachments
1	1	1
1	1	1